CLAIMS

[0060] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory device comprising:

a bit line disposed at a first level above a substrate;

a switching device disposed to second level above a substrate and below said first level, said switching device coupled to said bit line, said switching device being adapted to control a signal received from said bit line; and

a variable-state electronic device disposed at a third level above said first level, said variable state electronic device electrically coupled to said switching device to switchingly receive said signal therefrom.

2. The memory device of claim 1,wherein said switching device comprises a transistor.

3. The memory device of claim 2 further comprising a word line coupled to a gate of said transistor.

4. The memory device of claim 1, wherein said variable-state electronic device comprises a variable-conductivity memory cell.

5. The memory device of claim 1, wherein said variable-state electronic device comprises a variable-capacitance memory cell.

6. The memory device of claim 1, wherein said variable-state electronic device comprises a layer of chalcogenide material.

7. The memory device of claim 1, wherein said variable-state electronic device comprises:

a first electrode coupled to said switching device;

a second electrode disposed in spaced relation to said first electrode; and

a chalcogenic material disposed in a region between said first and second electrodes.

8. The memory device of claim 7, wherein said second electrode comprises a metallic material, said metallic material being adapted to release ions thereof into said chalcogenic material to produce a changed physical property of said chalcogenic material.

9. The memory device of claim 8, wherein said metallic material comprises tungsten.

10. The memory device of claim 8, wherein said metallic material comprises silver.

11. The memory device of claim 8, wherein said changed physical property comprises change conductivity.

12. The memory device of claim 8, wherein said changed physical property comprises changed optical reflectivity.

13. The memory device of claim 8, wherein said changed physical property comprises changed electrical capacitance.

14. The memory device of claim 1 further comprising a decoder circuit supported by said substrate, said decoder circuit adapted to control said switching device.

15. A memory device comprising:

a first electrode including a source of metal ions;

a second electrode disposed in spaced relation to said first electrode;

a resistance variable material disposed between said first electrode and said second electrode; and

switching means disposed below said first and second electrodes, said switching means adapted to couple said second electrode to a signal line disposed below said first and second electrodes.

16. The memory device of claim 15, wherein said switching means includes a transistor and wherein said transistor is adapted to be controlled by a word line disposed beneath said first and second electrodes.

17. The memory device of claim 15, wherein said signal line comprises a bit line.

18. An electronic device comprising:

a transistor having a first and second controlled terminal regions and a gate;

first and second conductors disposed above and electrically coupled to said first and second controlled terminal regions respectively;

a first signal line disposed above and coupled to said first conductor;

a first electrode disposed above and coupled to said second conductor;

a second electrode disposed in spaced relation to said first electrode; and

a region of material adapted to exhibit a changed physical property in response to a voltage applied between said first and second electrodes.

19. The electronic device of claim 18, wherein said region of material comprises a chalcogenic variable resistance material.

20. The electronic device of claim 18, wherein said second electrode comprises silver.

21. A memory device comprising:

a transistor coupled between a bit line and a first electrode;

a second electrode disposed in spaced relation to said first electrode and separated therefrom by an insulating region, said first and second electrodes being disposed above said transistor; and

a region of variable resistance material disposed between said first and second electrodes.

22. An integrated circuit memory device comprising:

an electrode structure disposed above a bit line and separated therefrom by a substantially non-conductive region;

first and second transistors electrically coupled to said bit line, said first and second transistors being adapted to switchingly electrically couple said bit line to second and third electrodes respectively, said second and third electrodes being disposed in spaced relation to one another and to said first electrode; and

a layer of variable resistance material disposed in a first region between said first and second electrodes and in a second region between said first and third electrodes.

23. The integrated circuit memory device of claim 22, wherein said third electrode is disposed between said first and second electrodes.

24. The integrated circuit memory device of claim 22, wherein said substantially nonconductive region comprises an insulating material.

25. The integrated circuit memory device of claim 24, wherein said insulating material comprises silicon nitride.

26. The integrated circuit memory device of claim 24, wherein said insulating material comprises silicon dioxide.

27. An integrated circuit memory device comprising:

electrode structure disposed above a bit line and separated therefrom by a region of insulating material;

first and second transistors electrically coupled to said bit line, said first and second transistors being adapted to switchingly electrically couple said bit line to second and third electrodes respectively, said second and third electrodes being disposed in spaced relation to one another and to said first electrode;

a layer of variable resistance material disposed in a first region between said first and second electrodes and in a second region between said first and third electrodes;

a word line decoder, said word line decoder being electrically coupled to respective gates of said first and second transistors;

a bit line decoder, said bit line decoder being electrically coupled to said bit line; and

electrode decoder, said electrode decoder being electrically coupled to said first electrode.

28. A method for storing a logical bit in a variable resistive memory, said method comprising:

coupling a bit line to a source of ground potential;

coupling a first electrode structure to a source of elevated potential;

activating a switching device, said switching device being coupled between said bit line and a second electrode, and thereby grounding said second electrode; and

detectably modifying a physical property of a material disposed between said first electrode structure and said second electrode.

29. The method of claim 28, wherein said switching device comprises a transistor.

30. The method of claim 28, wherein said act of detectably modifying a physical property comprises changing a conductivity of said

material disposed between said first electrode structure and said second electrode.

31. The method of claim 28, wherein said material disposed between said first electrode structure and said second electrode comprises a chalcogenic material.

32. The method of claim 31, wherein said chalcogenic material comprises silver.

33. A method for reading a logical bit out of a variable resistive memory, said method comprising:

coupling a bit line to a sensing circuit;

activating a switching device using a sub-write threshold voltage, said switching device being coupled between said bit line and a first electrode;

elevating a second electrode to the sub-write threshold voltage; and

sensing a physical property of a material disposed between said first electrode and said second electrode.

34. The method of claim 33, wherein said switching device comprises a transistor.

35. The method of claim 33, wherein said act of sensing a physical property comprises detecting a conductivity of said material disposed between said first electrode structure and said second electrode.

36. The method of claim 33, wherein said material disposed between said first electrode structure and said second electrode comprises a chalcogenic material.

37. The method of claim 36, wherein said chalcogenic material comprises silver.

38. A method for forming a memory integrated circuit comprising:

providing a substrate;

forming a transistor on said substrate;

forming a layer of insulating material over said transistor;

forming first and second conductors through said insulating material, said first and second conductors being coupled to a source and a drain of said transistor respectively;

forming a bit line coupled to one of said first and second conductors;

forming a first electrode coupled to the other of said first and second conductors;

forming a second electrode structure disposed in spaced relation to said first electrode; and

disposing a layer of chalcogenic material in a region between said first electrode and said second electrode structure.

39. The method of claim 38, further comprising the act of disposing a layer of insulating material over said bit line and below said second electrode structure.

40. The method of claim 39, wherein said act of disposing the layer of insulating material over said bit line and below said second electrode structure comprises disposing a layer of Borophosphosilicate glass over said bit line and below said second electrode structure.

41. The method of claim 38, wherein said act of forming said transistor on said substrate comprises:

forming a layer of insulating material over said substrate;

forming a layer of conductive material over said substrate;

doping said substrate to form said source and said drain of said transistor; and

coupling said layer of conductive material to a word line conductor.